CLAIMS

I claim:

1. A system for testing semiconductor circuits comprising:

a voltage vector system generating an output voltage vector, the power supply vector system configured to apply the output voltage vector to a drain and a source of a semiconductor circuit;

a current measuring system configured to measure a quiescent current provided by the voltage vector system to the drain and from the source of the semiconductor circuit; and

a controller coupled to the voltage vector system and the current measuring system, the controller receiving the output voltage vector and the quiescent current measurement and determining whether a variation of the quiescent current measurement exceeds a predetermined allowable variation.

2. The system of claim 1 wherein the controller further comprises a go/no-go system causing the power supply vector system to apply a maximum voltage to the drain of the semiconductor circuit and determining whether the quiescent current measured by the quiescent current measuring system exceeds a predetermined maximum allowable level.

3. The system of claim 1 wherein the controller further comprises an IDDQ variation monitor determining whether (|IDDQ(VCCmax) – IDDQ(VCCmin)|/(Min (IDDQ(VCCmax), IDDQ(VCCmin))) is less than a predetermined value.

4. The system of claim 1 wherein the semiconductor circuit is a field effect transistor semiconductor circuit.

5. The system of claim 1 further comprising an excitation voltage system applying an excitation voltage to the semiconductor circuit, and wherein the quiescent current is measured after the excitation voltage has been applied for a predetermined time.

6. A method for testing integrated circuits comprising:

providing an excitation voltage to a device;

providing a power supply voltage to the device;

measuring the quiescent power supply current of the device;

changing the power supply voltage to the device; and

determining whether a change in quiescent power supply current of the device exceeds a predetermined allowable change.

7. The method of claim 6 wherein the device is a field effect transistor.

8. The method of claim 6 wherein changing the power supply voltage to the device comprises changing the power supply voltage to one or more predetermined voltages.

9. The method of claim 6 wherein determining whether the change in quiescent power supply current of the device exceeds the predetermined allowable change comprises determining whether (|IDDQ(VCCmax) – IDDQ(VCCmin)|/(Min (IDDQ(VCCmax), IDDQ(VCCmin))) is less than a predetermined value.

10. The method of claim 6 wherein measuring the quiescent power supply current of the device comprises:

determining whether the quiescent power supply current exceeds a maximum predetermined value; and

stopping subsequent testing if the quiescent power supply current exceeds the maximum predetermined value.

11. The method of claim 6 further comprising generating notification data if the change in quiescent power supply current of the device exceeds the predetermined allowable change.

12. A method for testing integrated circuits comprising:

providing an excitation voltage to a device;

providing a power supply voltage to the device;

measuring the quiescent power supply current of the device; and

changing the power supply voltage to the device if the quiescent power supply current is less than a predetermined value.

13. The method of claim 12 further comprising stopping testing if the quiescent power supply current exceeds the predetermined value.

14. The method of claim 12 wherein measuring the quiescent power supply current of the device further comprises waiting a predetermined period of time before measuring the quiescent power supply current of the device.

15. The method of claim 12 wherein the device is a field effect transistor.